Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (currently amended) A circuit for addressing a memory, to which memory, independently from each other, input data can be written at ~~different~~ individual write addresses ~~with~~ at a first clock rate and ~~from which~~ output data can be read at different read addresses ~~with~~ at a second clock rate, ~~it being possible for the memory to be fed~~ wherein a write reset ~~pulse that~~ signal is supplied to the circuit, which reset signal resets the write address to an initial value, ~~and it being possible for the memory to be fed~~ wherein a read reset ~~pulse that~~ signal is supplied to the circuit, which read reset signal resets the read address to an initial value, wherein switching means are provided ~~in order to~~ , which derive the read reset ~~pulse~~ signal from the write reset ~~pulse~~ signal, and wherein the circuit includes an adjustable delay element producing a fixed temporal relationship of the read-out data with regard to a read-side start signal.

2. (currently amended) The circuit as claimed in claim of claim 1, wherein the circuit ~~comprises~~ includes a detector ~~set up in order~~ adapted to detect synchronization data from the input data ~~in order to generate~~ for generating the write reset ~~pulse~~ signal.

Claim 3 is cancelled.

4. (currently amended) The circuit ~~as claimed in claim 3~~ of claim 1~~,~~ ~~wherein the circuit has~~ includes a counter that is started ~~by~~ in dependence of the start ~~pulse~~ signal and, beginning from a start value, counts down ~~proceeding from a start value as far as~~ to an end value.

5. (currently amended) The circuit ~~as claimed in~~ of claim [4] 3, wherein the circuit ~~is provided with~~ includes a storage means, in which the present value of the counter is stored if a read-side reset ~~pulse occurs~~ signal is present.

6. (currently amended) The circuit ~~as claimed in claim 5~~ of claim 4, wherein a connection is provided between the storage means and the adjustable delay element, said connection being set up in order to write the stored value of the counter as a delay value to the adjustable delay element.

7. (currently amended) The circuit ~~as claimed in~~ of claim 1, wherein the switching means are ~~provided in order~~ adapted to detect from the write-side reset ~~pulse~~ signal a pulse edge that triggers the generation of a read-side reset ~~pulse~~ signal.

8. The circuit ~~as claimed in~~ of claim 1, wherein ~~provision is made of~~ counters are provided that generate the write and read address, respectively, of the memory.

9. The circuit ~~as claimed in claim 8~~ of claim 7, wherein the counters are clocked with the write and read clock signal, respectively.